Laboratory 2

(Due date: October 7th)

OBJECTIVES

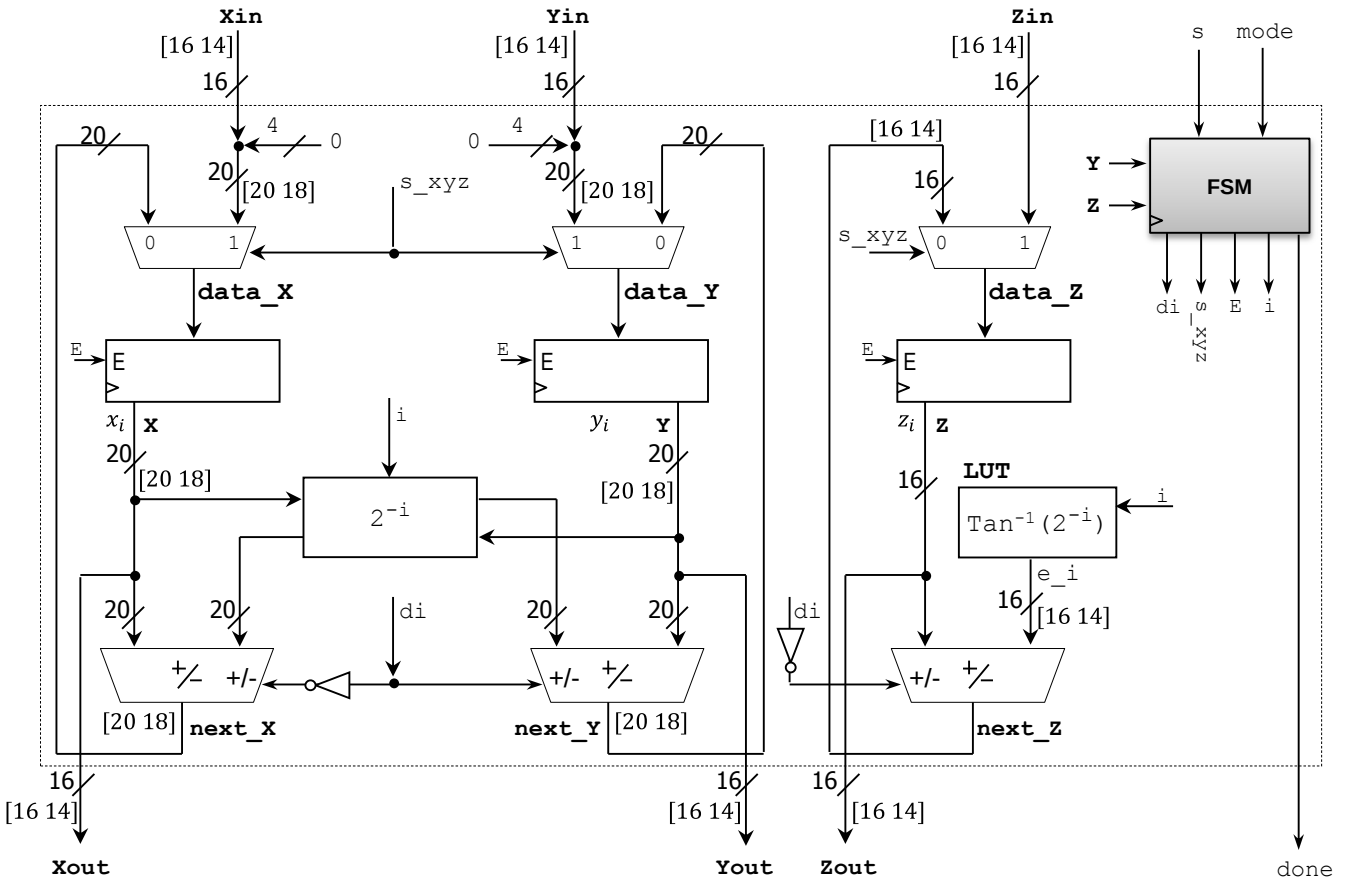
- ✓ Design of a dedicated circuitry for trigonometric functions (CORDIC) in fixed-point arithmetic: FSM + Datapath
- ✓ Test of the CORDIC circuit using fixed-point inputs/outputs.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a tutorial and a list of examples.

FIRST ACTIVITY (100/100)

- Circular CORDIC with 16 iterations. $i = 0, 1, 2, 3, \ldots 15$. $i = 0$ represents the initial conditions.
- **Input/Output Format**:
  - ✓ Xin, Yin, Zin: [16 14]
  - ✓ $Xout, Yout, Zout$: [16 14]
  - ✓ We restrict the inputs $x_0 = Xin, y_0 = Yin$ to $[-1,1)$. This means that only one integer bit is required. The reason we use 2 bits for the integer part is for consistency in the Input/Output format.
- **Internal format for x_i, y_i**: We use 4 extra bits (we first add four 0's to the LSB part), so that the format becomes [20 18].
- The CORDIC operations need up to 2 integer bits (this was determined by MATLAB simulation). Our formats satisfy this requirement.
- **Angles**: We use the format [16 14]. Units: radians.
- **Barrel shifters**: Feel free to use any code online (recommendation: `lpm_clshift` megafunction).
- **FSM**: You need to design a State Machine that controls the iteration index i, as well as the internal signals.
- Simulate it for the following cases. For each case verify that x_{16}, y_{16}, z_{16} reach the proper values.
  - ✓ Rotation Mode: $x_0 = 0, y_0 = 1/A_n, z_0 = \pi/6$.
  - ✓ Rotation Mode: $x_0 = 0, y_0 = 1/A_n, z_0 = -\pi/3$.
  - ✓ Vectoring Mode: $x_0 = y_0 = 0.8, z_0 = 0$
  - ✓ Vectoring Mode: $x_0 = 0.5, y_0 = 1, z_0 = 0$



XILINX ZYNQ SOC DESIGN FLOW:

- ✓ Create a new Vivado Project. Select the **ZYNQ XC7Z010-1CLG400C** device.
- ✓ Using the structural coding approach in VHDL: Instantiate the barrel shifter, multiplexors, LUT, FSM, and adder/subtractors into a top file. Synthesize your circuit (Run Synthesis).
- ✓ Write the VHDL testbench to properly test the circuit.
- ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your instructor.**

- Submit (as a .zip file) the generated files: VHDL code, and VHDL testbench to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

Instructor signature: _____ **Date:** _____